



PTO/SB/08A (10-01)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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2

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Complete if Known

Application Number 08/530,661

Application Number: 087530,001

Filing Date September 1, 2000

First Named Inventor

Group Art Unit 2814

Group A1 Unit 2614

Examiner Name D. Wille

<p style="text-align: center;"><i>(use as many sheets as necessary)</i></p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p>		<i>Complete if Known</i>	
Sheet	1	of	2
Attorney Docket Number			
5990LJS (95-0424.00/LJS)			

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

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Substitute for form 1449A/PTO				<i>Complete if Known</i>	
				Application Number	08/530,661
				Filing Date	September 20, 1995
				First Named Inventor	Keeth et al.
				Group Art Unit	2814
				Examiner Name	D. Wille
				Attorney Docket Number	5990 LIS (95-0424 00/LIS)
Sheet	2	of	2		

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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS				
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T ²
DW		European Search Report completed 26 February 2003 for European Application No. EP 03,001,319.		
		Asakura, M., "An Experimental 256-Mb DRAM with Boosted Sense-Ground Scheme," 29(11) IEEE Journal of Solid-State Circuits 1303-09 (Nov. 1994).		
		Denboer, Anthony, "Inside Today's Leading Edge Microprocessors," Semiconductor International (Feb. 1994).		
		Hamamoto, T., et al., "NAND-Structured Trench Capacitor Cell Technologies for 256 MB DRAM and Beyond," IEICE Transactions on Electronics, Institute of Electronics Information and Comm. Eng. Tokyo, JP, Vol. E78-C, NR. 7, pp. 789-796 (July 1995).		
		Sunouchi, K., et al., "A Surrounding Gate Transistor (SGT) cell for 64/256 Mbit DRAMs," EEDM 89 23 (1989), IEEE Inc., New York NY, pp. 2.1.1-2.1.4.		
		Watanabe, S., et al., "A Novel Circuit Technology with Surrounding Gate Transistors (SGTs) for Ultra High Density DRAM's" 30(9) IEEE Journal of Solid-State Circuits 960-70 (September 1, 1995).		

Examiner Signature	<i>Dwight Wille</i>	Date Considered	<i>20 Jan 04</i>
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